What is Claimed is:

1. A firmware hub comprising:

a random number generator to generate random bits, the random number generator including:

an interface circuitry coupled to an input/output controller hub to receive and output the random bits; and

a random number generation circuitry coupled to the interface circuitry to generate and output the random bits to the interface circuitry; and

a memory coupled to the random number generator to store one or more of system software and video software.

2. The firmware hub of claim 1 wherein the interface circuitry prevents outputting same random bits more than once.

3. The firmware hub of claim 1 wherein the random number generation circuitry generates random bits based on one or more of a semiconductor noise and a thermal noise.

4. The firmware hub of claim 1 wherein the random number generation circuitry includes:

a random bit source to generate and output the random bits;

a digital signal processor coupled to the random bit source to receive and process the random bits and output the processed bits to the interface circuitry; and

a control circuitry coupled to the random bit source and the digital signal processor to provide a control function to the random bit source and the digital signal processor.

5. The firmware hub of claim 1 wherein the interface circuitry includes:

an accumulator to receive and store the random bits output from the random number generation circuitry and output the stored random bits; and

a plurality of registers to assist in generation and reading of the random bits.

6. The firmware hub of claim 5 wherein the plurality of registers are selected from a group comprising a status register and a configuration register.

7. The firmware hub of claim 1 wherein the interface circuitry includes a status register to store a validity bit indicating whether valid random bits are available to output.

8. The firmware hub of claim 1 wherein the interface circuitry outputs random bits through a data register interface and sets the data register interface to a predetermined value when the data register interface is read.

9. The firmware hub of claim 1 wherein the random number generator outputs the random bits to the memory.

10. The firmware hub of claim 1 wherein the memory includes flash memory.

11. The firmware hub of claim 1 wherein the memory and the random number generator are integrated on a same chip.

12. The firmware hub of claim 1 wherein the interface circuitry indicates whether valid random bits are available to output.

13. The firmware hub of claim 1 wherein the random number generation circuitry generates random bits based on one or more of a semiconductor noise and a thermal noise.

14. A firmware hub comprising:

a memory to store basic input/output system software; and

a random number generator.

15. The firmware hub of claim 14, wherein the random number generator comprises:

random number generation circuitry to generate and output random bits, and

interface circuitry to receive and store random bits output by the random number generation circuitry and to output random bits, the interface circuitry to prevent outputting same random bits more than once.

16. The firmware hub of claim 15, wherein the interface circuitry indicates whether valid random bits are available to output.

17. The firmware hub of claim 16, wherein the interface circuitry comprises a status register to store a validity bit indicating whether valid random bits are available to output.

18. The firmware hub of claim 15, wherein the interface circuitry outputs random bits through a data register interface and sets the data register interface to a predetermined value when the data register interface is read.

19. The firmware hub of claim 15, wherein the random number generation circuitry generates random bits based on semiconductor or thermal noise.

20. The firmware hub of claim 15, wherein the interface circuitry comprises one or more registers to store random bits.

21. The firmware hub of claim 20, wherein the interface circuitry comprises a plurality of registers to store random bits and a multiplexer to output random bits from one of the registers at a time.

22. The firmware hub of claim 14, wherein the memory comprises flash memory.

23. The firmware hub of claim 14, wherein the memory and the random number generator are integrated on a same chip.

24. A chipset comprising:

(a) a memory controller hub;

(b) an input/output controller hub; and

(c) a firmware hub comprising:

(i) a memory to store basic input/output system software, and

(ii) a random number generator.

25. The chipset of claim 24, wherein the random number generator comprises:

random number generation circuitry to generate and output random bits, and

interface circuitry to receive and store random bits output by the random number generation circuitry and to output random bits, the interface circuitry to prevent outputting same random bits more than once.

26. The chipset of claim 25, wherein the random number generation circuitry generates random bits based on semiconductor or thermal noise.

27. The chipset of claim 25, wherein the interface circuitry indicates whether valid random bits are available to output.

28. The chipset of claim 27, wherein the interface circuitry comprises a status register to store a validity bit indicating whether valid random bits are available to output.

29. The chipset of claim 25, wherein the interface circuitry outputs random bits through a data register interface and sets the data register interface to a predetermined value when the data register interface is read.

30. The chipset of claim 25, wherein the interface circuitry comprises one or more registers to store random bits.

31. The chipset of claim 30, wherein the interface circuitry comprises a plurality of registers to store random bits and a multiplexer to output random bits from one of the registers at a time.

32. The chipset of claim 24, wherein the memory and the random number generator are integrated on a same chip.

33. The chipset of claim 24, wherein the memory comprises flash memory.

34. A computer system comprising:

(a) one or more processors;

(b) a memory controller hub;

(c) an input/output controller hub; and

(d) a firmware hub comprising:

(i) a memory to store basic input/output system software, and

(ii) a random number generator.

35. The computer system of claim 34, wherein the random number generator comprises:

random number generation circuitry to generate and output random bits, and

interface circuitry to receive and store random bits output by the random number generation circuitry and to output random bits, the interface circuitry to prevent outputting same random bits more than once.

36. The computer system of claim 35, wherein the random number generation circuitry generates random bits based on semiconductor or thermal noise.

37. The computer system of claim 35, wherein the interface circuitry indicates whether valid random bits are available to output.

38. The computer system of claim 35, wherein the interface circuitry comprises a status register to store a validity bit indicating whether valid random bits are available to output.

39. The computer system of claim 35, wherein the interface circuitry outputs random bits through a data register interface and sets the data register interface to a predetermined value when the data register interface is read.

40. The computer system of claim 35, wherein the interface circuitry comprises a plurality of registers to store random bits and a multiplexer to output random bits from one of the registers at a time.

41. The computer system of claim 34, wherein the memory comprises flash memory.

42. The computer system of claim 34, wherein the memory and the random number generator are integrated in a same chip.

43. A method comprising:

determining whether a random number generator has valid random bits available to output; and

reading the random bits from the random number generator.

44. The method of claim 43, wherein the determining comprises reading a validity bit from the random number generator.

45. The method of claim 43, wherein the determining comprises reading a validity bit from the random number generator, and wherein the reading random bits comprises reading the random bits during a same atomic read transaction while reading the validity bit.

46. The method of claim 43, comprising enabling the random number generator to generate random numbers.

47. The method of claim 43, comprising repeating the determining and the reading and forming a random number from read random bits.